



# **iCE40 Oscillator Usage Guide**

## **Technical Note**

FPGA-TN-02008 Version 1.4

September 2017

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# 1. Introduction

The iCE40™ family, specifically iCE40 Ultra™, iCE40 UltraLite™ and iCE40 UltraPlus™, features two on-chip oscillators. An ultra-low power 10 kHz oscillator is provided for Always-On applications and background polling that allow higher power processors to remain in power-down or sleep mode, conserving overall power consumption. A low power 48 MHz oscillator with output divider is provided for sensor management and pre-processing functions. These oscillators are intended for general clocking of internal logic and state machines.

## 1.1. Key Features

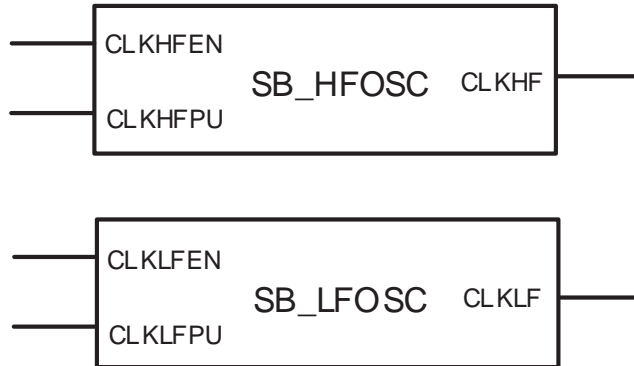
Two oscillators are available to users:

- SB\_LFOSC – Low Frequency Oscillator
- SB\_HFOSC – High Frequency Oscillator with output divider

## 2. On-Chip Oscillator Overview

You can access the two modules: SB\_LFOSC and SB\_HFOSC with enabled inputs and which you can dynamically control as shown in [Figure 2.1](#).

SB\_LFOSC runs at 10 kHz and SB\_HFOSC runs at maximum 48 MHz with output divider by 1, 2, 4 or 8. SB\_LFOSC and SB\_HFOSC provide internal clock sources to user designs. These clocks can directly route to the global clock network or to local fabric.



**Figure 2.1. On-Chip Oscillator**

### 3. I/O Port Description

**Table 3.1. SB\_HFOSC I/O**

Pin Name	Pin Direction	Description
CLKHFEN	I	Enabling CLKHF output to be oscillating. This does not stop the oscillator, but only disables the output.
CLKHF	O	Oscillator Clock Output.
CLKHFPU	I	Powering up the SB_HFOSC.

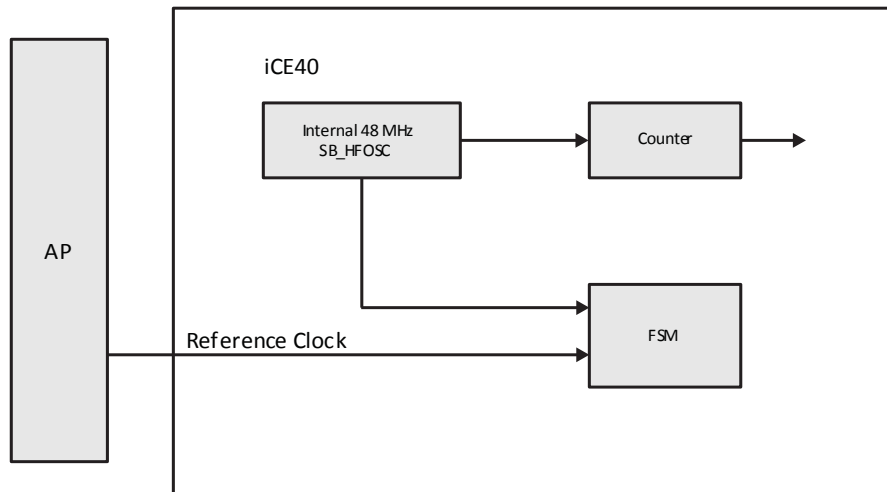
**Table 3.2. SB\_LFOSC**

Pin Name	Pin Direction	Description
CLKLFEN	I	Enabling CLKLF output to be oscillating. This does not stop the oscillator, but only disables the output.
CLKLF	O	Oscillator Clock Output.
CLKLFPU	I	Powering up the SB_LFOSC.

## 4. Connectivity Guideline

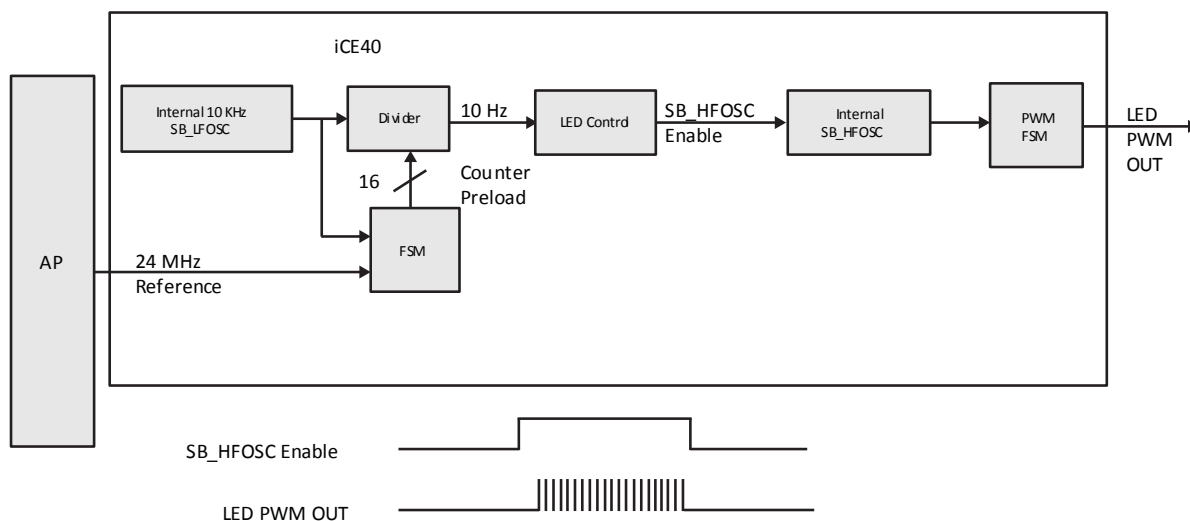
The SB\_HFOOSC and SB\_LFOOSC can be used as clock source. Their outputs are available for the user. They should be connected to the global clock network or local fabric. By default, the outputs will be routed to global clock network. To route to local fabric, see the examples in the [Appendix: Design Entry](#) section.

Note that Oscillator cannot provide accurate frequency. For applications that require more accuracy, it is recommended to use calibration circuit to support the oscillator used as clock source. [Figure 4.1](#) shows an example of the use of a reference clock that is only temporarily available for calibration.



**Figure 4.1. Oscillator Calibration Example**

The calibration circuit for Oscillator can be improved for the purpose of power saving as shown in [Figure 4.2](#). In this example, 10 kHz oscillator is always on. Calibrated divider provides timing for LED on-off. When LED is on, SB\_LFOOSC Enable turns on 48 MHz oscillator (SB\_HFOOSC turns on in two cycles). PWM FSM provides accurate PWM for LED. Power benefit is 48 MHz only when LED is on and minimum power when LED is off.



**Figure 4.2. Oscillator Used for Dynamic Clock Calibration That Can Be Used On Service LED**

## 5. Power Management Options

When disabled, the SB\_LFOSC and SB\_HFOSC are in standby mode by default and consume only DC leakage. It is suggested to always enable SB\_LFOSC and enable SB\_HFOSC after there is an activity detected and the products return to full power mode for data analysis/processing.

## Appendix: Design Entry

The following examples illustrate SB\_HFOSC and SB\_LFOSC usage with VHDL and Verilog.

### SB\_LFOSC Usage with Verilog

#### Synthesis Attributes

```
/* synthesis ROUTE_THROUGH_FABRIC = <value> */
```

Value:

0: Use dedicated clock network. Default option.

1: Use fabric routes.

#### Verilog Instantiation

```
SB_LFOSC OSCInst1 (  
  .CLKLFEN (ENCLKLF) ,  
  .CLKLFP (CLKLF_POWERUP) ,  
  .CLKLF (CLKLF)  
) /* synthesis ROUTE_THROUGH_FABRIC= [0|1] */;
```

### SB\_HFOSC Usage with Verilog

#### Synthesis Attributes

```
/* synthesis ROUTE_THROUGH_FABRIC = <value> */
```

Value:

0: Use dedicated clock network. Default option.

1: Use fabric routes.

#### Parameter Values

The SB\_HFOSC primitive contains the following parameter and their default values:

Parameter CLKHF\_DIV = 2'b00 : 00 = div1, 01 = div2, 10 = div4, 11 = div8 ; Default = "00"

#### Verilog Instantiation

```
SB_HFOSC OSCInst0 (  
  .CLKHFEN (ENCLKHF) ,  
  .CLKHFPU (CLKHF_POWERUP) ,  
  .CLKHF (CLKHF)  
) /* synthesis ROUTE_THROUGH_FABRIC= [0|1] */;  
Defparam OSCInst0.CLKHF_DIV = 2'b00;
```



## Technical Support Assistance

Submit a technical support case via [www.latticesemi.com/techsupport](http://www.latticesemi.com/techsupport).

## Revision History

Date	Version	Change Summary
September 2017	1.4	Fixed the port name of SB_LFOSC and SB_HFOSC modules.
		Changed document number from TN1296 to FPGA-TN-02008.
		Updated document template.
		Removed clock generation logic information from the <a href="#">Connectivity Guideline</a> section.
June 2016	1.3	Updated <a href="#">Introduction</a> section. Added iCE40 UltraPlus.
April 2015	1.2	Updated <a href="#">Connectivity Guideline</a> section. Added example of clock generation logic.
		Updated <a href="#">Technical Support Assistance</a> section.
January 2015	1.1	Added support for iCE40 UltraLite.
June 2014	01.0	Initial release.



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